

In re application of:

Confirmation No.:

4782

Christopher R. Risucci

Art Unit:

2183

Appl. No.:

09/925,314

Examiner:

Henry Tsai

Filed:

August 10, 2001

Atty. Docket:

1778.0180000 (0106.00US)

For:

System and Method of Controlling Software Decompression Through

**Exceptions** 

## **Second Supplemental Information Disclosure Statement**

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Sir:

Listed on accompanying Form PTO-1449 are documents that may be considered material to the examination of this application, in compliance with the duty of disclosure requirements of 37 C.F.R. §§ 1.56, 1.97 and 1.98.

Applicant has listed publication dates on the accompanying PTO-1449 based on information presently available to the undersigned. However, the listed publication dates should not be construed as an admission that the information was actually published on the date indicated.

Applicant reserves the right to establish the patentability of the claimed invention over any of the information provided herewith, and/or to prove that this information may not be prior art, and/or to prove that this information may not be enabling for the teachings purportedly offered.

This statement should not be construed as a representation that a search has been made, or that information more material to the examination of the present patent application

does not exist. The Examiner is specifically requested not to rely solely on the material submitted herewith.

This Information Disclosure Statement is being filed under 37 C.F.R. § 1.97(b) before the mailing of a first Office Action after the filing of a request for continued examination under 37 C.F.R. § 1.114. No statement or fee is required.

Copies of documents AK1, AL1, AM1, AN1, AO1, AP1, AQ1, AR1, AK2, AN2, AO2, AP2, AQ2, AR2, AN3, AO3, and AP3 are provided herewith. In accordance with 37 C.F.R. § 1.98(a)(2), no copies of U.S. patents and patent application publications cited on the accompanying Form PTO-1449 are provided.

It is respectfully requested that the Examiner initial and return a copy of the enclosed Form PTO-1449, and indicate in the official file wrapper of this patent application that the documents cited thereon have been considered.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLOSTEIN & FOX P.L.L.C.

Virgil L. Beaston

Attorney for Applicant Registration No. 47,415

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Page 1 of 3

**FORM PTO-1449** 

## SECOND SUPPLEMENTAL **INFORMATION DISCLOSURE STATEMENT**

ATTY. DOCKET NO. 1778.0180000 APPLICATION NO. 09/925,314 FIRST NAMED INVENTOR Christopher R. Risucci FILING DATE **ART UNIT** August 10, 2001 2183

			U.S. PA	TENT DOCUMENTS		12		
EXAMINER		DOCUMENT				SUB-	RADPANT	
INITIAL	1	NUMBER	DATE	NAME	CLASS	CLASS	PILING DATE	
	AA1	3,794,980	02/1974	Cogar et al.				
	AB1	3,811,114	05/1974	Lemay et al.				
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INTIAL	AK1	EP 0 073 424 A2	03/1983	Europe	CEAGG	OLAGO	N/A	
	AL1	EP 0 239 081 B1	09/1995	Europe			N/A	
	AM1	EP 0 368 332 B1	09/1997	Europe			N/A	
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	AN1	Cobb, Paul, "TinyRISC: a MIPS-16 embedded CPU core," Presentation for Microprocessor For 13 slides (7 pages) (October 22-23, 1996).						
	AO1	U.S. Utility Patent Application No. 09/702,112, inventors Jensen, M., et al., filed October 30, 200 (not published) (67 pages).						
	AP1	U.S. Utility Patent Application No. 09/702,115, inventors Jensen, M., et al., filed October 30, 2000 (not published) (71 pages).						
	AQ1	U.S. Reissue Patent Application No. 10/066,475, inventor Edward Colles Nevill, filed February 2002 (based on U.S. Pat. No. 6,021,265, issued February 1, 2000) (9 pages).						
	AR1	inventor Edward C	olles Nevill, fil	ebruary 1, 2002, in U.S. Reed February 1, 2002 (base				
		February 1, 2000)	(15 pages).				,	

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance

and not considered. Include copy of this form with next communication to Applicant.

Page 2 of 3

ATTY. DOCKET NO. APPLICATION NO. 09/925,314

FIRST NAMED INVENTOR Christopher R. Risucci

FILING DATE

ART UNIT

2183

SECOND SUPPLEMENT SECOND DISCLOSURE STATEMENT TRADENTS

NITIAL   NUMBER	EXAMINER			U.S. PA	TENT DOCUMENTS			
AA2				DATE	NAME	CLASS		FILING DATE
AC2 4,724,517 02/1988 May, Michael D.  AD2 4,777,594 10/1988 Jones et al.  AE2 4,782,441 11/1988 Inagami et al.  AE2 5,132,988 07/1992 Sakamura et al.  AG2 5,241,636 08/1993 Kohn, Leslie D.  AH2 5,327,566 107/1994 Forsyth, Mark A.  AI2 5,355,460 10/1994 Eickemeyer et al.  AJ2 5,556,974 04/1996 Church et al.  FOREIGN PATENT DOCUMENTS  DOCUMENT NUMBER DATE COUNTRY CLASS CLASS TRANSLATIO  AK2 EP 0 449 661 B1 11/1995 Europe Y  AL2 AM2  OTHER (Including Author, Title, Date, Pertinent Pages, etc.)  AN2 Gwennap, Linley, "VLIW: The Wave of the Future?: Processor Design Style Could Be Faster, Cheaper Than RISC," Microprocessor Report, Vol. 8, No. 2, pp. 18-21 (February 14, 1994).  Kurosawa, K., et al., "Instruction Architecture For A High Performance Integrated Prolog Processo IPP," Logic Programming: Proceedings of the Fifth International Conference and Symposium (August 15-19, 1988), MIT Press, Cambridge, MA, Vol. 2, pp. 1506-1530 (1988).  AP2 IBM Technical Disclosure Bulletin, "Patchable Read-Only Storage and Other Patchable Functions, Vol. 27, Issue 6, pp. 3496-3499 (November 1, 1984) (4 pages).  IBM Technical Disclosure Bulletin, "Patch RAM Load Technique," Vol. 27, Issue 6, pp. 3597-3598 (November 1, 1984) (3 pages).		AA2	4,507,728	03/1985	Sakamoto et al.			
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AK2 EP 0 449 661 B1 11/1995 Europe N  AL2 Y  AM2 Y  OTHER (Including Author, Title, Date, Pertinent Pages, etc.)  AW2 Gwennap, Linley, "VLIW: The Wave of the Future?: Processor Design Style Could Be Faster, Cheaper Than RISC," Microprocessor Report, Vol. 8, No. 2, pp. 18-21 (February 14, 1994).  Kurosawa, K., et al., "Instruction Architecture For A High Performance Integrated Prolog Processor IPP," Logic Programming: Proceedings of the Fifth International Conference and Symposium (August 15-19, 1988), MIT Press, Cambridge, MA, Vol. 2, pp. 1506-1530 (1988).  AP2 IBM Technical Disclosure Bulletin, "Patchable Read-Only Storage and Other Patchable Functions, Vol. 27, Issue 6, pp. 3496-3499 (November 1, 1984) (4 pages).  AQ2 IBM Technical Disclosure Bulletin, "Patch RAM Load Technique," Vol. 27, Issue 6, pp. 3597-3598 (November 1, 1984) (3 pages).	EXAMINER INITIAL			DATE	COUNTRY	CLASS		TRANSLATION
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OTHER (Including Author, Title, Date, Pertinent Pages, etc.)  AN2  Gwennap, Linley, "VLIW: The Wave of the Future?: Processor Design Style Could Be Faster, Cheaper Than RISC," <i>Microprocessor Report</i> , Vol. 8, No. 2, pp. 18-21 (February 14, 1994).  Kurosawa, K., et al., "Instruction Architecture For A High Performance Integrated Prolog Processor IPP," Logic Programming: Proceedings of the Fifth International Conference and Symposium (August 15-19, 1988), MIT Press, Cambridge, MA, Vol. 2, pp. 1506-1530 (1988).  AP2  IBM Technical Disclosure Bulletin, "Patchable Read-Only Storage and Other Patchable Functions, Vol. 27, Issue 6, pp. 3496-3499 (November 1, 1984) (4 pages).  AQ2  IBM Technical Disclosure Bulletin, "Patch RAM Load Technique," Vol. 27, Issue 6, pp. 3597-3598 (November 1, 1984) (3 pages).		AL2						Yes
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Gwennap, Linley, "VLIW: The Wave of the Future?: Processor Design Style Could Be Faster, Cheaper Than RISC," <i>Microprocessor Report</i> , Vol. 8, No. 2, pp. 18-21 (February 14, 1994).  Kurosawa, K., et al., "Instruction Architecture For A High Performance Integrated Prolog Processo IPP," <i>Logic Programming: Proceedings of the Fifth International Conference and Symposium (August 15-19, 1988)</i> , MIT Press, Cambridge, MA, Vol. 2, pp. 1506-1530 (1988).  BM Technical Disclosure Bulletin, "Patchable Read-Only Storage and Other Patchable Functions, Vol. 27, Issue 6, pp. 3496-3499 (November 1, 1984) (4 pages).  BM Technical Disclosure Bulletin, "Patch RAM Load Technique," Vol. 27, Issue 6, pp. 3597-3598 (November 1, 1984) (3 pages).		AIVIZ						No
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August 10, 2001

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ATTY. DOCKET NO. 1778.0180000

FIRST NAMED INVENTOR Christopher R. Risucci

FILING DATE August 10, 2001 ART UNIT 2183

APPLICATION NO 09/925,314

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Page 3 of 3

EXAMINER			U.S. PA	ATENT DOCUMENTS		·	E TROOMANTE !
INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB- CLASS	FILING DATE
	AA3	5,574,873	11/1996	Davidian, Gary G.			
	AB3	5,732,234	03/1998	Vassiliadis et al.			10-
	AC3	6,266,765 B1	07/2001	Horst, Robert W.			
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	AE3	2001/0021970 A1	09/2001	Hotta et al.			
	AF3	2004/0054872 A1	03/2004	Nguyen et al.			
	AG3						
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			FOREIGN	PATENT DOCUMENTS		.1 .	_ t
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB- CLASS	TRANSLATION
	AK3		1	N			Yes
	AL3						Yes
							No Yes
	AM3						No
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	AN3	NEC Data Sheet, NEC Electronics Co	orporation 200	00) (76 pages).		•	essor (Copyright
	AO3	NEC Electronics Co	orporation 200 re's no risk in	the future for RISC," <i>Com</i>	nputer Design,	Vol. 28, No	
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	AO3	Ross, Roger, "Ther (November 13, 198) NEC User's Manua	re's no risk in (9).	the future for RISC," <i>Com</i>			. 22, pp. 73-75
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**EXAMINER**: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.